

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Li Attorney Docket: 2003 P 54557 US
Filed: Herewith Examiner: TBD
Serial No.: TBD Art Unit: TBD
For: Transistor with Doped Gate Dielectric

Mail Stop: Patent Application
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

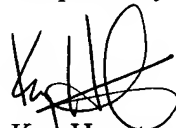
INFORMATION DISCLOSURE STATEMENT

Dear Sir:

The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed concurrently with the patent application.

Respectfully submitted,



Kay Houston
Attorney for Applicant
Reg. No. 38,495

February 3, 2004

Date

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			Filing Date	HEREWITH
			First Named Inventor	Li
			Art Unit	TBD
			Examiner Name	TBD
Sheet	1	of	Attorney Docket Number	2003 P 54557 US

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1	INUMIYA, S., <i>et al.</i> , "Fabrication of HfSiON Gate Dielectrics by Plasma Oxidation and Nitridation, Optimized for 65nm node Low Power CMOS Applications," 2003 Symposium on VLSI Technology Digest of Technical Papers, pp. 18-19, Document No. 4-89114-035-6/03.	
	2	WOLF, S., "Silicon Processing for the VLSI Era: Diffusion in Silicon" pp. 336-339.	

Examiner Signature	Date Considered
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